USN | | | | | | | | | | |

06CS81

Eighth Semester B.E. Degree Examination, June / July 2013
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO question from each part.***

PART - A

1 a. Define Computer Architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. Assume a disk subsystem with the following components and MTTF.
i) 10 Disk, each rated at 1000000 – hours MTTF ii) 1 SCSI controller 500,000 – hours MTTF iii) 1 power supply 200,000 – hours MTTF iv) 1 Fan 200,000 – hours MTTF v) 1 SCSI cable 1,000,000 – hours MTTF. Using the simplifying assumptions that the life times are exponentially distributed and that failure are independent. Compute the MTTF of the system as a whole. **(04 Marks)**

c. We will run two applications on this dual Pentium but the resource requirements are not equal. The first application needs 80% of the resources and the other only 20% of the resources.
i) Given that 40% of the first application is parallelizable, how much speed up would you achieve with that application if run in isolation?
ii) Given that 99% of the second application is parallelizable, how much speed up would this application observe if run in isolation?
iii) Given that 40% of the first application is parallelizable, how much overall system speed up would you observe if you parallelized it?
iv) Given that 99% of the second application is parallelizable, how much overall system speedup would you get? **(08 Marks)**

2 a. What is pipelining? List pipeline hazards. Explain any one in detail. **(10 Marks)**

b. With a neat diagram, explain the classic five stage pipeline for RISC processor. **(10 Marks)**

3 a. Mention the techniques used to reduce branch costs. Explain static and dynamic branch prediction used for same. **(08 Marks)**

b. What is data dependencies? Mention the different types of data dependencies. Explain Name dependencies with example between two instructions. **(06 Marks)**

c. What is correlating predictors? Explain with examples. **(06 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP using multiple issues. **(08 Marks)**

b. Write a note on value prediction. **(04 Marks)**

c. Mention the key issues in implementing advanced speculation techniques. Explain. **(08 Marks)**

PART - B

5 a. Explain any two hardware primitives to implement synchronization, with example. **(10 Marks)**

b. Explain the basic schemes for enforcing Coherence in a shared memory multiprocessor system. **(10 Marks)**

6 a. Briefly explain four basic Cache optimization methods. **(10 Marks)**

b. Assume we have a computer where the Clocks Per Instruction (CPI) is 1.0. When all memory accesses hit in the Cache. The only data accesses are loads and stores and these total 50% of the Instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%. How much faster would the computer be if all the Instructions were Cache hits? **(10 Marks)**

7 a. Which are the major categories of advanced optimization of Cache performance? Explain any one in detail. **(10 Marks)**

b. Explain internal organization of 64MB DRAM, with neat figure. **(05 Marks)**

c. Briefly explain how memory protection is enforced via virtual memory. **(05 Marks)**

8 a. Explain in detail the hardware support for preserving exception behavior during speculation. **(10 Marks)**

b. Explain Intel IA – 64 Architecture. **(10 Marks)**

*****